**Application No.: 10/602,878** 

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1-3. (Cancelled)

4. (Currently amended) A method for carrying out a burn-in test on a great number of

semiconductor devices that have been formed on a semiconductor wafer, each said device

including a gate oxide film between a substrate and a gate electrode, the gate electrode being

connected to a metal interconnect, wherein the method comprises the step of exposing the wafer

to an electromagnetic wave as an alternating current wave and placing so as to place an electric

field with a predetermined intensity on the gate oxide film of each said device on the wafer,

thereby carrying out the burn-in test on the devices.

5. (Original) The method of claim 4, comprising the steps of: sensing a voltage stress

imposed on the gate oxide film of each said device while the wafer is being exposed to the

electromagnetic wave; and controlling the intensity of the electric field, which is represented by

the electromagnetic wave generated, so that the voltage stress sensed as being imposed on the

gate oxide film falls within a preset threshold value range.

6. (Original) The method of claim 5, wherein the voltage stress, which has been sensed

as being imposed on the gate oxide film, comprises a forward voltage stress and a reverse

voltage stress, and wherein the electric field intensity of the electromagnetic wave generated is

controlled so that the forward and reverse voltage stresses imposed on the gate oxide film fall

within first and second preset threshold value ranges, respectively, the second range being lower

than the first range.

2

**Application No.: 10/602,878** 

7-9. (Cancelled)

10. (Currently amended) A method for carrying out a burn-in test on a great number of semiconductor devices that have been formed on a semiconductor wafer, each said device including a gate oxide film between a substrate and a gate electrode, the gate electrode being connected to a metal interconnect, wherein the method comprises the step of exposing the wafer to an electric field as an alternating current wave and, thereby setting the electric field placed on the gate oxide film of each said device on the wafer to a predetermined intensity, thereby earrying so as to carry out the burn-in test on the devices.

11. (Original) The method of claim 10, comprising the steps of: sensing a voltage stress imposed on the gate oxide film of each said device while the wafer is being exposed to the electric field; and controlling the intensity of the electric field generated so that the voltage stress sensed as being imposed on the gate oxide film falls within a preset threshold value range.

12. (Original) The method of claim 11, wherein the voltage stress, which has been sensed as being imposed on the gate oxide film, comprises, a forward voltage stress and a reverse voltage stress, and wherein the intensity of the electric field generated is controlled so that the forward and reverse voltage stresses imposed on the gate oxide film fall within first and second preset threshold value ranges, respectively, the second range being lower than the first range.

13-15. (Cancelled)

**Application No.: 10/602,878** 

16. (Original) A method for carrying out a burn-in test on a great number of semiconductor devices that have been formed on a semiconductor wafer, each said device including a gate oxide film between a substrate and a gate electrode, the gate electrode being connected to a metal interconnect, the method comprising the steps of: exposing the wafer to an electric field that has been generated as a direct current wave from a conductive plate; and loading and unloading the wafer into/from a space, where the electric field generated from the conductive plate exists, to expose the wafer to the electric field intermittently, whereby the wafer is exposed to an alternating-current electric field to carry out the burn-in test on the devices.